REMARKS/ARGUMENTS

Claims 1-14 were previously pending in the application. Claims 1-14 are canceled; claims 15-49 are added herein. Assuming the entry of this amendment, claims 15-49 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 3 of the final office action, the Examiner rejected claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Myers in view of Matsumoto. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

New Claims 15, 33, and 49

New claim 15 is directed to apparatus for generating a delayed output digital audio signal from an input digital audio signal. The apparatus comprises a first delay module and a second delay module. The first delay module applies a first amount of delay to the input digital audio signal to generate a partially delayed digital audio signal, where the first delay module selects the first amount of delay from a plurality of available first delay values separated from one another by increments at a first resolution level. The second delay module applies a second amount of delay to the partially delayed digital audio signal to generate the delayed output digital audio signal, where the second delay module selects the second amount of delay from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first resolution level. The Applicant submits that the cited references do not teach or even suggest such a combination of features.

In Fig. 20, for example, Myers teaches that an audio input signal at input terminal 110 is applied to a plurality of time delays 118 connected in series, where the delay amount of each time delay 118 is controllable. See column 13, lines 38-43. The output of each time delay 118 is then separately delayed by a corresponding pair of interaural time delay circuits 120-134, where the delay amount of each interaural time delay circuit is also controllable. See column 13, lines 43-55. Significantly, however, Myers provides no teaching that the delay amount applied by each time delay 118 is selected "from a plurality of available first delay values separated from one another by increments at a first resolution level," where the delay amount applied by each interaural time delay circuit 120-134 is selected "from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first resolution level." There is no teaching in Myers at all related to the resolution of the different delay amounts.

In rejecting previously pending claims 1-14 in paragraph 3, the Examiner cited Fig. 4 of Matsumoto as teaching "adding two delays (fig. 4), one being a digital integer delay (DLY 40 with 20 ms), and the other being a digital fractional delay (DLY 32, 33, having value of 0.7 ms)." In making this rejection, the Applicant submits that the Examiner confused the concept of delay magnitude with the concept of delay resolution.

The magnitude of delays refers to the absolute size of the delay values, while the resolution of delays refers to the smallest difference in magnitude between any two available delay values. For example, consider the following two sets of available delay values: S1 = {10 ms, 11 ms, 12 ms} and S2 = {100 ms, 101 ms, 102 ms}. While the magnitude of each delay value in set S1 is smaller than the magnitude of each delay value in set S2, the two sets have the same resolution (i.e., 1 ms}.

Consider, further, the following set of available delay values: S3 = {10 ms, 20 ms, 30 ms}. Here, the magnitude of each delay value in set S3 is smaller than the magnitude of each delay value in set S2, but the resolution of set S3 (i.e., 10 ms) is greater than the 1-ms resolution of set S2.

These examples demonstrate the differences between the concepts of magnitude and resolution.

While it may be true that Matsumoto teaches a series combination of two delays having different magnitudes (e.g., the 0.7-ms magnitude of DLY 32, 33 is smaller than the 20-ms magnitude of DLY 40), there is no teaching in Matsumoto related to the resolutions of the delay values supported by those delay modules. Similarly, Myers also fails to provide any teachings related to the resolutions of the different delay modules taught in that reference.

For all these reasons, the Applicant submits that new claim 15 is allowable over the cited references. For similar reasons, the Applicant submits that new claims 33 and 49 are allowable over the cited references. Since the rest of the claims depend variously from claims 15 and 33, it is further submitted that those claims are also allowable over the cited references.

New Claims 16, 30, 34, and 46

According to new claim 16, the total range of the plurality of available second delay values at the second resolution level is substantially equal to each increment at the first resolution level. None of the cited references provides any teachings similar to this feature. The Applicant submits that this provides additional reasons for the allowability of claim 16 and also claims 30, 34, and 46 (and therefore claims 31-32 and 47-48) over the cited references.

New Claims 17, 30, 35, and 46

According to new claim 17, the first delay module comprises a buffer and a switch. The buffer receives and stores a plurality of digital values corresponding to the input digital audio signal such that each position in the buffer corresponds to a different one of the plurality of available first delay values. The switch has a plurality of input ports and an output port, wherein each input port is connected to receive a different digital value stored in the buffer, and the switch presents one of the received digital values at its output port based on a first delay control signal.

While time delays 118 of Myers may be said to form an example of a buffer similar to the buffer of claim 17, Myers does not teach an example of the switch of claim 17. The Applicant submits that this provides additional reasons for the allowability of claim 17 and also claims 30, 35, and 46 (and therefore claims 18, 31-32, 36, and 47-48) over the cited references.

New Claims 19, 30, 37, and 46

According to new claim 19, the second delay module comprises a plurality of digital filters, configured in parallel, and switch circuitry. Each digital filter applies a different one of the plurality of available second delay values, while the switch circuitry selects, based on a second delay control signal, one of the digital filters to provide the second amount of delay. None of the cited references provides any teachings similar to these features. The Applicant submits that this provides additional reasons for the allowability of claim 19 and also claims 30, 37, and 46 (and therefore claims 20-22, 31-32, 38 and 47-48) over the cited references.

New Claims 20, 31, 38, and 47

According to new claim 20, the digital filters are all-pass filters having different phase shift values. None of the cited references provides any teachings similar to this feature. The Applicant submits that this provides additional reasons for the allowability of claim 20 and also claims 31, 38, and 47 over the cited references.

New Claims 21 and 31

According to new claim 21, the switch circuitry comprises an input switch adapted to receive and forward the partially delayed digital audio signal to only the selected digital filter. None of the cited references provides any teachings similar to this feature. The Applicant submits that this provides additional reasons for the allowability of claim 21 and also claim 31 (and therefore claim 22) over the cited references.

New Claims 22 and 31

According to new claim 22, the switch circuitry further comprises an output multiplexer having a plurality of input ports and an output port, wherein each input port is connected to a different digital filter, and the output multiplexer is adapted to present the output from the selected digital filter at its output port. None of the cited references provides any teachings similar to these features. The Applicant submits that this provides additional reasons for the allowability of claim 22 and also claim 31 over the cited references.

New Claims 24, 31, 40, and 47

According to new claim 24, the control module comprises a look-up table (LUT) storing data that maps 3D positions to interaural delays, and the control module is adapted to receive a specified 3D position value, retrieve a corresponding interaural delay value from the LUT based on the specified 3D position value, and generate the first and second delay control signals on the retrieved interaural delay value. None of the cited references provides any teachings similar to these features. The Applicant submits that this provides additional reasons for the allowability of claim 24 and also claims 31, 40, and 47 over the cited references.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

Date: 6/30/05

Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)